In the claims:

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims

1. (Original) A method of modulating the flatband voltage of a high-k dielectric material of a semiconductor device, comprising the steps of:

depositing the high-k dielectric material on a surface; and

controllably modulating the flatband voltage of the high-k dielectric material by annealing the high-k dielectric material under controlled annealing parameters.

2. (Original) The method of claim 1, wherein the controlled annealing parameters include at least one of: annealing temperatures; annealing times; annealing gases; and number of anneals.

3. (Original) The method of claim 2, wherein the annealing includes controlling the temperature of anneals between about 400°C to about 1000°C.

4. (Original) The method of claim 3, wherein the annealing includes a plurality of anneals with a different annealing gas in each anneal.

5. (Original) The method of claim 4, wherein the annealing gases include at least one of: O_2, N_2, H_2 and NH_3.

6. (Original) The method of claim 5, wherein the annealing includes controlling the annealing time between 10 seconds to 60 seconds.

7. (Original) The method of claim 1, wherein the step of controlling modulating includes changing the flatband voltage by at least 0.3V.

8. (Original) The method of claim 1, wherein the step of controllably modulating includes modulating the high-k dielectric material for P-channel devices to a first

value and the high-k dielectric material for N-channel devices to a second value different from the first value.

9. (Original) The method of claim 8, wherein the step of modulating the high-k dielectric material for P-channel devices to a first value includes annealing with N_2.

10. (Original) The method of claim 9, further comprising preventing exposure of the high-k dielectric material for N-channel devices to the N_2 during the step of modulating the high-k dielectric material for P-channel devices.

11. (Original) A method for forming a semiconductor chip, comprising the steps of:

depositing a high-k dielectric film;

annealing to modify the flatband voltage of the high-k dielectric film to a first value for a first set of devices on the chip; and

annealing to modify the flatband voltage of the high-k dielectric film to a second value, different than the first value, for a second set of devices on the chip.

12. (Original) The method of claim 11, wherein the first set of devices are N-channel devices and the second set of devices are P-channel devices.

13. (Original) The method of claim 12, wherein the step of annealing to modify the flatband voltage of the high-k dielectric film includes masking the N-channel devices and subjecting the P-channel devices to annealing with N_2.

14. (Original) The method of claim 13, further comprising subjecting both the N-channel devices and the P-channel devices to an annealing with NH_3 and an annealing with O_2.

15. (Original) The method of claim 14, further comprising subjecting both the N-channel devices and the P-channel devices to an annealing with H_2.

16. (Original) The method of claim 15, further comprising controlling annealing temperature during each annealing to control the flatband voltage of the high-k dielectric film.

17. (Original) The method of claim 16, further comprising controlling annealing time during each annealing to control the flatband voltage of the high-k dielectric film.